**Digital Semiconductor**

# DECchip 21130 PCI Integrated Graphics and Video Accelerator

## Compatible Memory Devices: An Application Note

Order Number: EC-QLEGB-TE

**June 1995**

This application note provides a list of EDO and non-EDO DRAM devices that have been tested and qualified for use with the DECchip 21130 Integrated Graphics/Video Accelerator. When the device is revised, all the parts listed will be retested and this document will be updated. As new DRAMs become available from suppliers, we will test them and issue new qualification reports. Graphics hardware and systems engineers can use this application note to design graphics controllers or motherboard-based graphics subsystems using the DECchip 21130.

**Revision/Update Information:** This document supersedes the *DECchip 21130 PCI Integrated Graphics and Video Accelerator Compatible Memory Devices: An Application Note* (EC-QLEGA-TE).

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## Frame Buffer Configurations

The DECchip 21130 is designed to work with a minimum of two and a maximum of eight 256K × 16 DRAMs, representing minimum 1MB and maximum 4MB frame buffer configurations, respectively. The minimum frame buffer configuration of 1MB (two DRAMs) has a 32-bit-wide data path and depth of 256K (one bank). The minimum *high-performance* frame buffer configuration of 2MB has a 64-bit-wide data path, uses four DRAMs, and is also 256K (one bank) deep. The maximum frame buffer configuration adds a second bank of four DRAMs (eight DRAMs, total) on a 64-bit-wide data path for a total depth of 512K, in two banks.

| Frame Buffer Configuration | Frame Buffer Size | Total 256Kx16 DRAM Required | Data Path Width | Frame Buffer Depth | Number of Banks |
|---|---|---|---|---|---|
| Minimum | **1MB** | **2** | **32 bits** | **256K** | **1** |
| Minimum High Performance | **2MB** | **4** | **64 bits** | **256K** | **1** |
| Maximum High Performance | **4MB** | **8** | **64 bits** | **512K** | **2** |

**Note**

When in VGA mode or when the VAFC port is active, the frame buffer operates in 32-bit mode regardless of the actual amount of memory installed in the system. DRAMs wired to the upper 32 bits of frame buffer data path are not accessed in these modes.

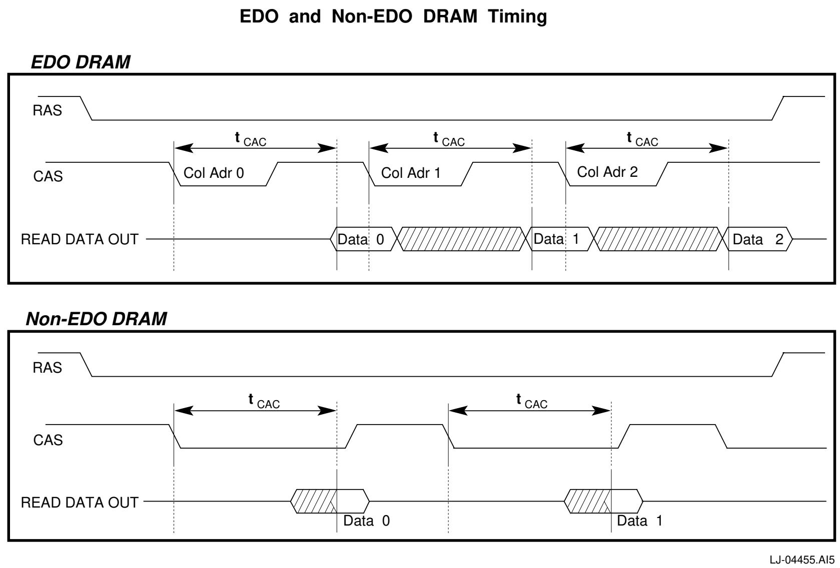
Software may set frame buffer width to *32-bit mode* when a 64-bit frame buffer is present, but must not set 64-bit width when only a 32-bit frame buffer is installed. At power-up, the memory controller operates as a 32-bit frame buffer configuration regardless of the actual amount of memory attached to the frame buffer interface.

## EDO DRAM Versus Non-EDO DRAM

The extended data-out (EDO) feature is an enhancement to normal fast-page-mode DRAMs for improved data bandwidth. DRAMs without the feature normally turn off their data output buffers (on read cycles) when CAS is deasserted, even if OE (output enable) stays asserted. An EDO DRAM, on the other hand, continues to access the column location and will drive data out even after CAS deasserts. This permits a read access to continue even after CAS goes high (see Figure 1). Compared to an equivalent-speed, non-EDO DRAM, the EDO part can substantially shorten its page-mode cycle time because CAS assertion (low time) no longer need be longer than column access time (tCAC).

Shorter EDO column-access cycles translate into higher bandwidth; a typical non-EDO DRAM might cycle at 25 MHz (40 ns), yielding peak system bandwidth of 200MB/s, while otherwise-equivalent EDO parts can run at 40 MHz for a total bandwidth of 320MB/s.

**Figure 1: Timing Diagram**




## Using Non-EDO DRAM with the DECchip 21130

The DECchip 21130 memory controller is optimized for use with EDO DRAMs to take advantage of the superior bandwidth of those devices. Timing diagrams in the *DECchip 21130 PCI Integrated Graphics and Video Accelerator Technical Reference Manual* show timing for EDO DRAMs used for frame buffer memory. However, both Revision C (DC7538C) and Revision E (DC7538E) versions of the 21130 work with non-EDO DRAMs as well. This lets the customer make price/performance decisions, rather than forcing a particular DRAM type into the design. In addition, it provides flexibility so customers can easily adapt to rapidly changing supply situations in the volatile DRAM market. The following sections detail system-level considerations for use of non-EDO DRAMs with both versions of the 21130.

### Using Non-EDO DRAMs with Revision C (DC7538C)

This version of the 21130 has no specific adaptations for the use of non-EDO DRAMs. However, it works reliably with a wide variety of non-EDO DRAMs provided the memory clock (MemClk) is set to an appropriate frequency for the timing requirements of the DRAM devices being used. This reliability has been confirmed by extensive tests with many different kinds of non-EDO DRAMs on a standard evaluation board (see Table 2).

During a read cycle to frame buffer DRAMs, the DECchip 21130 (Revision C) samples data one MemClk after the trailing edge of CAS, when data is guaranteed to be valid from EDO DRAMs (see Figure 1). With non-EDO DRAMs, read data will be driven to a valid state only while CAS is asserted, provided CAS assertion time is equal to, or longer than, the column access time (tCAC). After CAS deassertion, DRAM data will no longer be actively driven to the 21130; however, the data will remain on the lines for a long time, electronically speaking. Because there are only low leakage currents in the parts' I/Os, and no pull-up or pull-down resistors on the signals, the voltage level driven onto the data lines will be stable for many microseconds, or until a new memory cycle drives new data onto the lines. By comparison, sampling of the data value takes place 15 ns to 20 ns (one MemClk period) after active driving ceases, orders of magnitude sooner.

To confirm the conclusions of this analysis, we tested a variety of non-EDO DRAMs over wide ranges of supply voltage and MemClk frequencies. Table 2 shows reliable operation and excellent margins for the 21130 part working with many different non-EDO DRAMs installed on the reference design board.

For the most reliable operation with non-EDO DRAMs, MemClk should be set so the period of one cycle is equal to or greater than the DRAM's specified tCAC (column access time), plus some allowance for transition times. For example, the 70-ns KM416C256BJ (Samsung) has a tCAC specified at 18 ns; adding 2 ns for transition times and clock skew suggests a MemClk period of 20 ns (MemClk frequency of 50 MHz).

### Using Non-EDO DRAMs with Revision E (DC7538E)

Revision E (DC7538E) of the 21130 has a modification to make non-EDO DRAM cycles run faster, and to ensure maximum operating reliability with all suitable non-EDO DRAMs. This entails setting a bit in the *PCI clock control register* to enable the optimized timing. In addition, software may need some way of identifying which variety of DRAM is installed on the graphics card.

Non-EDO DRAMs need a longer CAS assertion time to ensure valid read data is accessed and driven onto the data lines before CAS deassertion tristates (turns off) the data outputs. This requirement is accommodated in the Revision C 21130 by simply slowing down MemClk. This has the side effect of lengthening all other portions of the memory cycle as well, which is *not* required for non-EDO DRAMs. In addition, it slows the clock to the graphics accelerator.

Revision E optimizes memory timing for non-EDO DRAMs by only lengthening the time of CAS assertion. This permits, for 70-ns non-EDO DRAMs, the default MemClk frequency of 80 MHz to be maintained. In addition, Revision E (in *non-EDO DRAM* mode) samples read data at the end of CAS assertion rather than a cycle later. This ensures reliable operation with any non-EDO DRAM.

Software can select the appropriate DRAM mode by using the *fast page enable* bit (bit 4) of the *PCI clock control register*. Sense of the bit is:

0 = EDO DRAM mode (this is the power-up default value)

1 = non-EDO DRAM (fast page) mode

If a product line plans on using both EDO and non-EDO varieties of DRAM, the software must have some means of knowing which variety is installed on the graphics card. This can be done either by loading DRAM-specific variants of BIOS into the graphics BIOS ROM, or by using one of the two available generic sense pins on the 21130 that are sampled at power-up. A pull-up or pull-down resistor on the pin can be used to set a power-up value, which signals the type of DRAM installed on the card.

## DRAM Qualification Testing

Both EDO and non-EDO 256K × 16 DRAM devices were tested in the DECchip 21130 reference design board over a range of supply voltages and MemClk operating frequencies. Temperature margining was not performed as part of these tests.

Parts were tested across the voltage range from 4.0 V to 6.0 V. At each voltage, the system's MemClk was varied from 25 MHz to the upper frequency limit at which diagnostic software began to detect failures (nominal MemClk is 80 MHz, the design target frequency for operating 60-ns EDO DRAMs). Note that both the DECchip 21130 and the DRAMs are being exercised by the diagnostics across these voltage and frequency ranges, so failures at the corners of the range may be due to complex interactions between the DRAMs and the DECchip 21130 device, and are not necessarily due to the DRAMs alone.

The parts were installed on a DECchip 21130 (DC7538C) reference design board, which was vertically installed in a DECpc XL590 system. The board was tested at room temperature (approximately 25$^{0}$C), with mostly convective airflow. Display resolution was set to 800×600. The DECchip 21130 full-diagnostic software routine was set to loop continuously, and MemClk frequency was increased until failures were detected. MemClk speed was set using the internal programmable MEMCLK PLL. No parts failed at the low frequency point of 30 MHz. **Note** that Table 1 and Table 2 are currently applicable to the **Revision C** version of DECchip 21130; tests will be rerun for the **Revision E** (DC7538E) version and this report will be reissued at that time.

**Table 1: Tested EDO DRAMs - Maximum MemClk Rate Before Failure (MHz)**

| Vendor | P/N | Speed (ns) | Vcc=4.0 Volts | Vcc=5.0 Volts | Vcc=6.0 Volts |
|---|---|---|---|---|---|
| Micron | MT4C16270DJ-6 | 60 | 81 | 91 | >100 |
| Micron | MT4C270DJ-7 | 70 | 84 | 97 | >100 |
| Samsung | KM416C254BJ-7 | 70 | 91 | 95 | 95 |
| NEC | 424210A-60 | 60 | 88 | 90 | 90 |
| Mosel Vitelic | V53C16258HK50 | 50 | 81 | 88 | 93 |
| Hitachi | HM5142655CLJ6 | 60 | 72 | 84 | 93 |
| Mitsubishi | M5M44265CJ-7S | 70 | 86 | 91 | 93 |
| ETRON | EM614163A-60 | 60 | | 87* | |

* Note: ETRON DRAMs were only tested with DC7538A prototype, at 5.0 V

**Table 2: Tested Non-EDO DRAMs - Maximum MemClk Rate Before Failures**

| Vendor | P/N | Speed (ns) | Vcc=4.0 Volts | Vcc=5.0 Volts | Vcc=6.0 Volts |
|---|---|---|---|---|---|
| Hitachi | HM514260AJ7 | 70 | 67 | 77 | 84 |
| Toshiba | TC514260BJ-70 | 70 | 67 | 72 | 74 |
| NEC | 424260-70 | 70 | 75 | 88 | 97 |
| Mitsubishi | M5M44260CJ-6 | 60 | 84 | 91 | 91 |
| OKI | M514260B-60J | 60 | 77 | 83 | 88 |
| OKI | M514260B-70J | 70 | 74 | 81 | 84 |
| Samsung | KM416C256BJ-7 | 70 | 94 | 97 | 99 |

## Performance Implications of Reduced-Speed MemClk

Designs using the Revision C version of the 21130 usually have to reduce MemClk frequency to operate with non-EDO DRAMs. To quantify the performance consequences of MemClk frequency reduction, we ran tests using the standard Ziff-Davis 1994 graphics benchmark, while varying MemClk from 30 MHz to 90 MHz. The results show that performance does not vary linearly with MemClk frequency and, in general, will vary only a small amount for relatively large changes in clock rate. For example, using a typical 70-ns non-EDO DRAM might entail reducing MemClk from the EDO default rate of 80 MHz down to 50 MHz, a reduction of over 35%; however, the resulting performance reduction is less than 10%.

Designs using Revision E of the 21130 will take even less of a performance hit when using non-EDO DRAMs. By setting the *fast page enable* bit, no changes need to be made to MemClk frequency for 70-ns DRAMs. The extra time added to the page-mode cycle reduces peak frame buffer bandwidth somewhat, but the reduction is less than that resulting from non-EDO DRAM use with Revision C parts. In addition, other memory timing is unchanged, and the graphics accelerator continues to run at full speed. When tests quantifying performance impact of non-EDO DRAM use with Revision E parts are complete, those results will be included in an updated version of this application note.

## Using 1Mb DRAMs (256K x 4) with the DECchip 21130

In some cases, for economic or availability reasons, a designer may want to consider using earlier-generation 256K $\times$ 4 devices for frame buffer memory. Although no actual hardware tests have validated the feasibility of this approach, our analysis of specifications for a number of these parts indicate there should be no problem making such a system work reliably.

Designers should keep in mind that all 1Mb DRAMs are non-EDO devices, so the guidelines for non-EDO design provided in this application note should be followed. In addition, there will be greater loading on the 21130 signal pins driving address and control signals to the frame buffer, since there will be 4 times as many devices for a given-size frame buffer (1MB frame buffer takes 8 DRAMs, while a 2MB frame buffer will require 16 devices). Do not attempt configurations of 4MB frame buffers using 1Mb DRAMs (32 parts).

To compensate for the additional loading, some extra time should be added to the non-EDO clock speed calculation, to allow for slower transitions of address and control signals driven by the 21130. We highly recommend that all configurations using 1Mb DRAMs be thoroughly tested, over a range of voltages and MemClk speeds, before deciding on a final MemClk frequency.

## Technical Support and Ordering Information

### Technical Support

If you need technical support or help deciding which documentation best meets your needs, call the Digital Semiconductor Information Line:

| | |
|---|---|
| United States and Canada | **1–800–332–2717** |
| TTY (United States only) | **1–800–332–2515** |
| Outside North America | **+1–508–568–6868** |

### Ordering Associated Digital Semiconductor Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

| Title | Order Number |
|---|---|
| DECchip 21130 PCI Integrated Graphics and Video Accelerator Technical Reference Manual | EC–QD2QB–TE |
| DECchip 21130 PCI Integrated Graphics and Video Accelerator Evaluation Board Design Example: An Application Note | EC–QHV4B–TE |