Digital Semiconductor

DECchip 21171 Core Logic Chipset

Product Brief

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Description

The DECchip 21171 core logic chipset provides a cost-effective solution for designing high-performance, uniprocessor systems using Digital's Alpha 21164 microprocessor. The chipset includes an interface to a 32- or 64-bit PCI local bus and control and data paths for a 21164, memory, and external third-level backup cache (Bcache).

The chipset gives the system designer flexibility in building the memory and I/O subsystem, and requires minimal discrete logic on the module.

The chipset uses two unique gate arrays:

- The DECchip 21171-CA control, I/O interface, and address (CIA) chip in a 383-pin pin gate array (PGA) package.
- The DECchip 21171-BA data switch (DSW) chip in a 208-pin plastic quad flat pack (PQFP) package.

Features

The DECchip 21171 core logic chipset enables the highest performance of client systems in the computer industry. Some features are:

- Central processor unit
  - Supports the Alpha 21164 microprocessor
- Components
  - One DECchip 21171-CA (CIA)
  - Four DECchip 21171-BA (DSW)
- Data paths
  - 64-bit, ECC-protected data path between CIA and DSW
  - 128-bit ECC-protected data path between 21164 and DSW
  - 128- or 256-bit ECC-protected data path between DSW and memory arrays
- Timing
  - Supports all 21164 clock frequencies
  - Supports system clock frequencies up to 33 MHz
  - PCI clock, cache, and memory clock periods are integer multiples of the 21164 clock period
- Bcache
  - Cache size from 2 to 16MB
  - Write-back, ECC-protected
  - Third-level cache for Alpha 21164 microprocessor
- Memory
  - Supports up to 8GB of ECC-protected physical memory
  - Industry-standard single in-line memory module (SIMM) configurations
- High-performance PCI
  - 64-bit multiplexed address and data
  - 64-bit PCI address handling
  - Scatter-gather map support
  - No glue logic required to connect PCI-compliant devices

DECchip 21171 Core Logic Chipset — System Overview

The DECchip 21171 core logic chipset consists of the CIA chip and four DSW chips (Figure 1).

DECchip 21171-CA (CIA) — The CIA provides control functions to main memory, the DSWs, and part of the I/O data path. It also acts as a bridge to the 64-bit PCI bus.

DECchip 21171-BA (DSW) — The DSW is bit-slice ASIC. Four are used to provide the data path between the 21164, main memory, Bcache, CIA, and part of the I/O data path.

MEMDATA Bus — The 256-bit MEMDATA bus provides an ECC-protected data path between the four DSWs and the memory arrays. Each DSW bit-slice connects to 64 bits of the MEMDATA bus.

IOD Bus — The 64-bit IOD bus provides an ECC-protected data path between the CIA and DSW chips.

SYS Bus — The SYS bus contains address, data, and command signal lines and connects the 21164 to the CIA and DSWs. The SYS bus is the 21164 interface bus with several additional signals to handle DMA transactions through the CIA and DSWs.

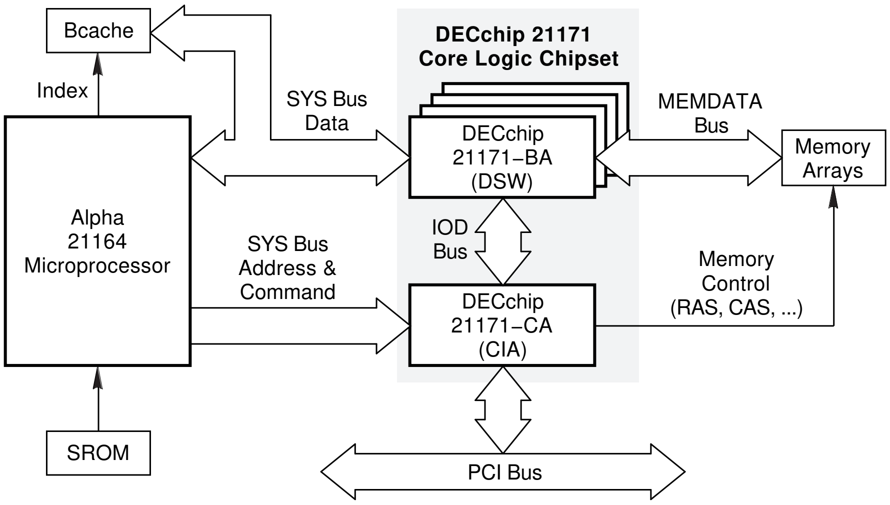
Memory — Systems built with the DECchip 21171 core logic chipset can support up to 8GB of memory. The chipset supports the following industry-standard SIMMs in the memory arrays:

1M × 36
2M × 36
4M × 36
8M × 36

To build a system, the following additional components are required:

- Alpha 21164 microprocessor
- Bcache
- Memory arrays
- SROM (for 21164)
- Input clock (for 21164)
- Support logic
  - PCI interrupt controller
  - PCI arbiter
  - Reset logic
  - Flash ROM (for PALcode and initialization instructions)
- PCI peripheral devices
- Phase-locked loop (PLL) for system clocks

Figure 1 DECchip 21171 Core Logic Chipset System Block Diagram



DECchip 21171-CA (CIA) Microarchitecture

The CIA provides control functions to main memory and the PCI interface. The CIA includes the following major functional logic blocks (Figure 2).

Instruction and Address Logic — This logic accepts commands from the 21164 and directs instructions to either the memory port or the I/O port.

A 3-entry 21164 instruction queue provides buffering in the event that the memory and I/O ports are busy.

A flush address register is also provided to allow DMA read and write operations to interrogate the Bcache for the most recent data.

Memory Logic — The memory logic provides the row and column address for the supported memory banks and all memory control functions (RAS, CAS, write enable, and so on). In addition, the memory logic provides control signals to the DSW to initiate memory data transactions.

I/O Address Logic — The I/O address logic handles I/O read and write addresses. The decode logic extracts the PCI address from the 21164 dense or sparse address space encoding, and generates PCI I/O read or write addresses and passes them to the PCI data path logic. The I/O logic can also increment the current address during each data cycle. The incremented address provides a pointer to the next data item to be transferred to or from the I/O read or write buffers.

A 3-entry I/O address queue together with a single-entry current address register allow four I/O write operations to be outstanding. The DSW chip provides four corresponding I/O write data buffers.

PCI Data Path Logic — The data path logic provides the interface to the 64-bit PCI bus and contains a portion of the data path control logic. Its major functions are to provide:

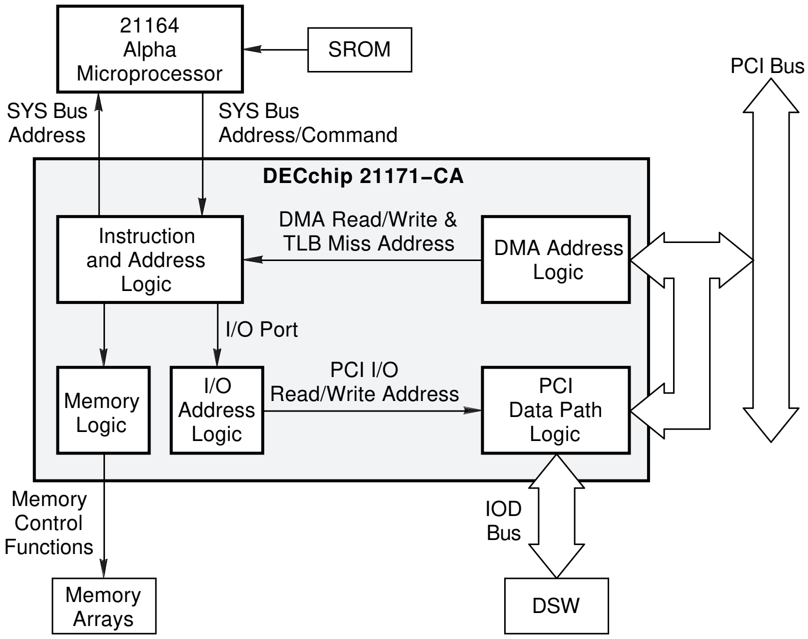
- ECC generation on data transactions to the DSW
- ECC check and correction on data transactions from the DSW
- I/O read and write addresses to the PCI bus
- Buffers for all I/O and DMA read and write data transactions

DMA Address Logic — The DMA address logic converts PCI addresses to 21164 memory address space. Two address conversion methods are provided.

- A direct path where a base offset is concatenated with the PCI address
- A scatter-gather map, which maps any 8KB PCI page to any 8KB memory space page

The scatter-gather map translation look-aside buffer (TLB) has eight entries, with each entry containing four consecutive page table entries (PTEs).

Figure 2 DECchip 21171-CA (CIA) Block Diagram



DECchip 21171-BA (DSW) Microarchitecture

The DSW provides bidirectional data paths between the 21164, the memory arrays, and the CIA (Figure 3). Four DSW bit-slice chips provide the complete data path.

The majority of the DSW logic comprises data buffers and multiplexers. DSW control is implemented with decode logic and state machines. Data flow is directed through the DSW by the CIA, using two encoded control fields. The DSW contains the following major functional logic blocks.

Victim Buffer — This logic has a 4-entry buffer to contain victim data during a 21164 memory read transaction that generates a victim. Victim data is saved in the buffer, allowing the read transaction to fetch read data from memory and send it to the 21164. Later, the victim data is written to memory.

Memory Interface — The memory data out register buffers either 21164 victim data to memory or DMA write data to memory.

The memory data in register accepts 21164 memory read data. The DSW clocks the register on optimum 15-ns clocks to minimize memory latency.

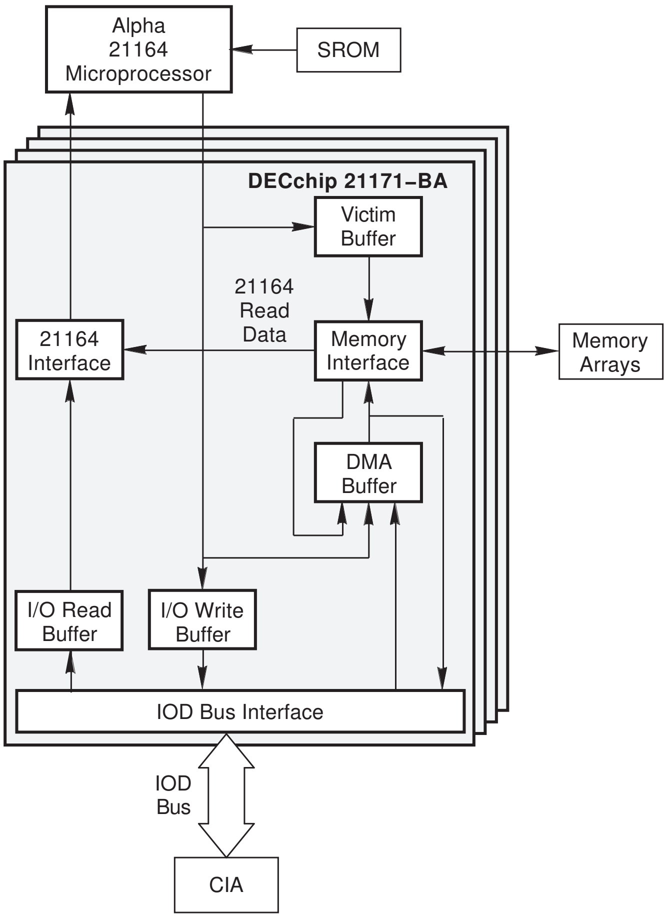
I/O Write Buffer — The I/O write buffer consists of four 32-byte buffers. The four buffers allow the chipset to sustain maximum bandwidth on a large copy operation from memory, through the 21164, to I/O space.

I/O Read Buffer — The 32-byte I/O read buffer is used to assemble the 128-bit data required by the 21164 from the 64-bit IOD bus (CIA-DSW interface) data.

DMA Read and Write Buffers — The DMA read and write buffers consist of two identical buffers (DMA buffer 0 and DMA buffer 1). Each buffer consists of three single-entry 64-byte data buffers to hold data from memory, Bcache, and the PCI bus.

When a buffer is written, its data valid bits are asserted. The valid bits are used to select the appropriate read or write data.

Figure 3 DECchip 21171-BA (DSW) Block Diagram



DECchip 21171-CA Characteristics

Characteristic	Specification
Power supply	Vss 0.0 V Vdd 5.0 V ±5%
Storage temperature range	–55°C to 125°C
Power dissipation @ Vdd = 5.25 V and Frequency = 33 MHz	2.75 W maximum
Package	383-pin pin gate array (PGA)

DECchip 21171-BA Characteristics

Characteristic	Specification
Power supply	Vss 0.0 V Vdd 5.0 V ±5%
Storage temperature range	–55°C to 125°C
Power dissipation @ Vdd = 5.25 V and Frequency = 33 MHz	1.0 W maximum
Package	208-pin plastic quad flat pack (PQFP)

For More Information

To learn more about the availability of the DECchip 21171 Core Logic Chipset, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

1-800-332-2717
1-800-332-2515 (TTY)

Outside North America, call:

+1-508-568-6868

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