DECchip 21140 PCI Fast Ethernet LAN Controller

Data Sheet

Order Number: EC–QC0BB–TE

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1 DECchip 21140 Overview

The DECchip 21140 PCI Fast Ethernet LAN Controller (21140) supports the peripheral component interconnect (PCI) bus. It provides a direct interface connection to the PCI and adapts easily to most other standard buses. The 21140 software interface and data structures are optimized to minimize the host CPU load and to allow for maximum flexibility in the buffer descriptor management. The 21140 contains large onchip FIFOs, so no additional onboard memory is required.

1.1 General Description

The 21140 interfaces with the PCI bus using onchip control and status registers (CSRs), and a shared CPU memory area that is set up mainly during initialization. This minimizes the processor involvement in the 21140 operation during normal reception and transmission. The 21140 is compliant with the *PCI Local Bus Specification*, Revision 2.0. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without needing to repeat a fetch from shared memory.

On the network side, the 21140 provides two ports: a serial (SRL) 10-Mb/s port and a media independent interface/symbol (MII/SYM) 100-Mb/s port. The 10-Mb/s port provides a direct interface to the external 10-Mb/s front-end decoder (ENDEC). The 100-Mb/s port supports two operational modes: a direct interface to the external 100-Mb/s ENDEC and a full implementation of the MII standard. The 21140 includes the onchip physical coding sublayer (PCS) and the scrambler for efficient 100BASE-T (CAT5 cable) implementation. It is also capable of functioning in a full-duplex environment for both the 10-Mb/s and 100-Mb/s ports.

1.2 Features

The 21140 has the following features:

- Offers a single-chip Fast Ethernet controller for PCI local bus:
  - Provides a direct interface to PCI bus
  - Supports two network ports: 10-Mb/s and 100-Mb/s
- Supports full-duplex operation on both 10-Mb/s and 100-Mb/s ports
- Contains large independent receive and transmit FIFOs; no additional onboard memory required
- Provides standard 100-Mb/s MII supporting CAT3 unshielded twisted-pair (UTP), CAT5 UTP, shielded twisted-pair (STP) and fiber cables
- Contains onchip scrambler and PCS for CAT5 to significantly reduce cost of 100BASE-T solutions
- Supports MII management functions
- Includes a powerful onchip DMA with programmable burst size providing for low CPU utilization
- Implements unique, patent-pending intelligent arbitration between DMA channels to minimize underflow or overflow
- Supports PCI clock speed range from 25 to 33 MHz
- Supports either big or little endian byte ordering
- Implements JTAG-compatible test-access port with boundary-scan pins
- Supports IEEE 802.3, ANSI 8802-3, and Ethernet standards
- Offers a unique, patented solution to Ethernet capture-effect problem
- Contains a variety of flexible address filtering modes (including perfect, hash tables, inverse perfect, and promiscuous):
  - 16 perfect addresses (normal or inverse filtering)
  - 512 hash-filtered addresses
  - 512 hash-filtered multicast addresses and one perfect address
  - Pass all multicast
  - Promiscuous
- Provides external and internal loopback capability on both ports

- Contains 8-bit, general-purpose, programmable register and corresponding I/O pins
- Provides serial MicroWire interface for Ethernet address external ROM
- Provides LED support for various network activity indications
- Implements low-power, 3.3-V complementary metal-oxide semiconductor (CMOS) process technology; interfaces to 5.0-V logic environment

1.3 Microarchitecture

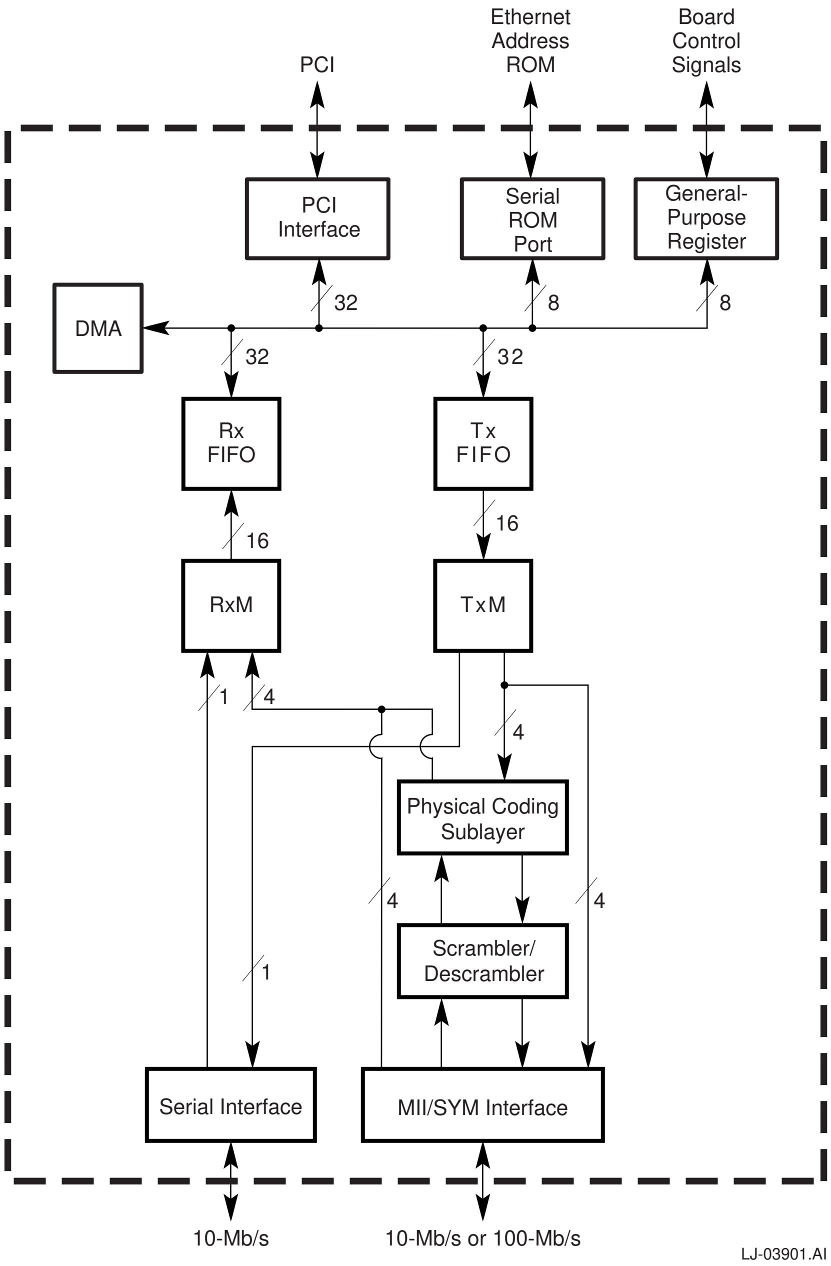
The following list describes the 21140 hardware components, and Figure 1 shows a block diagram of the 21140.

- PCI interface—Includes all interface functions to the PCI bus; handles all interconnect control signals, and executes PCI direct memory access (DMA) and I/O transactions
- DMA—Contains dual receive and transmit controller; supports bursts of up to 32 longwords; handles data transfers between CPU memory and onchip memory
- FIFOs—Contains two FIFOs for receive and transmit; supports automatic packet deletion on receive (runt packets or after a collision) and packet retransmission after a collision on transmit
- TxM—Handles all CSMA/CD[1] MAC[2] transmit operations, and transfers data from transmit FIFO to the ENDEC for transmission
- RxM—Handles all CSMA/CD receive operations, and transfers the data from the ENDEC to the receive FIFO
- Physical coding sublayer—Implements the encoding and decoding sublayer of the 100BASE-TX (CAT5) specification including the squelch
- Scrambler/descrambler—Implements the twisted-pair physical layer medium dependent (TP-PMD) scrambler/descrambler scheme
- General-purpose register—Enables software to use for input or output functions

[1] Carrier-sense multiple access with collision detection
[2] Media access control

- Serial interface—Provides a 7-wire conventional interface to the Ethernet ENDEC components
- MII/SYM interface— Provides a full MII signal interface and a direct interface to the 100-Mb/s ENDEC for CAT5
- Serial ROM—Provides a direct interface to the MicroWire Ethernet address ROM and other system parameters

Figure 1 DECchip 21140 Block Diagram



2 Pinout

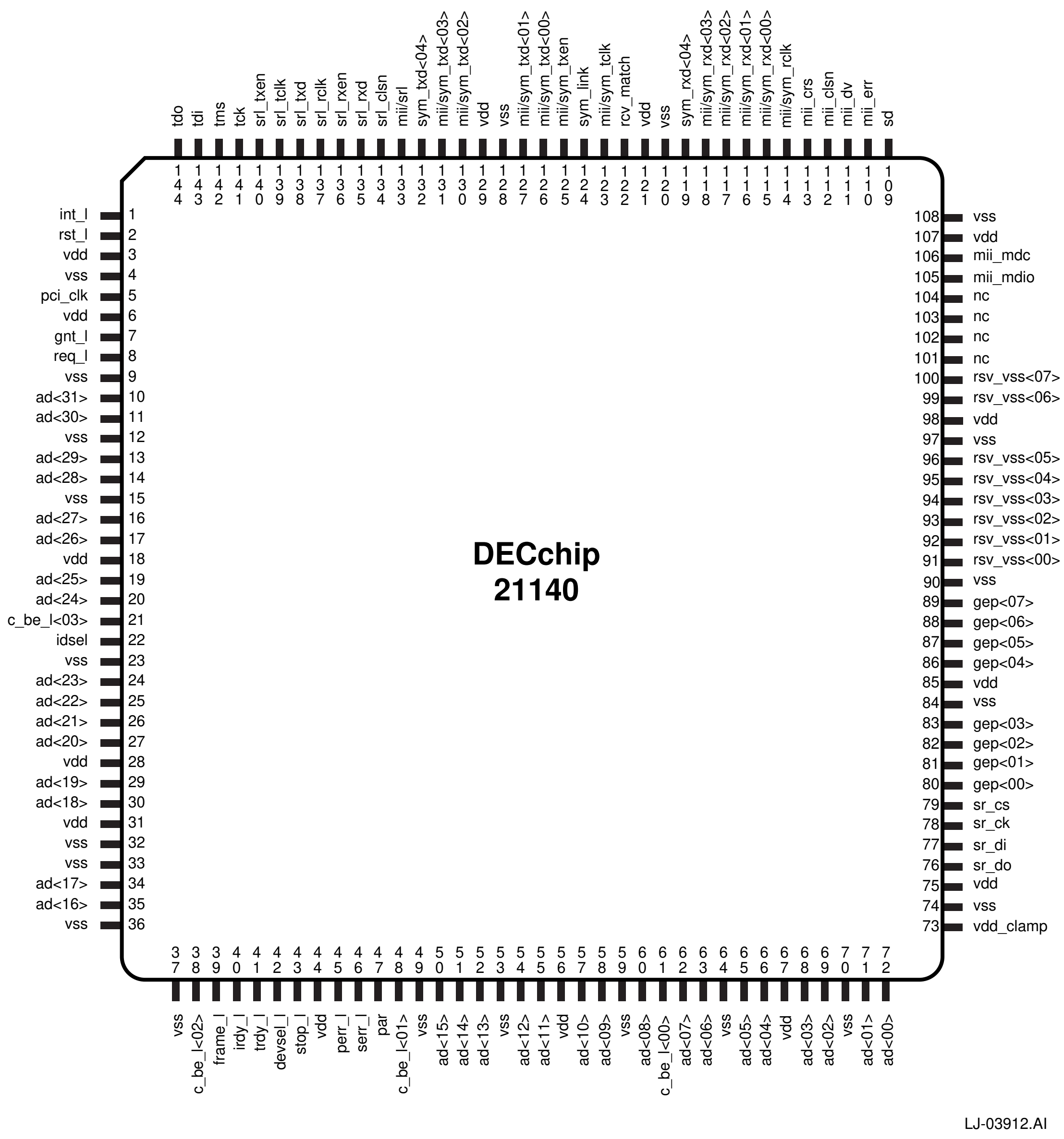
The 21140 is packaged in a 144-pin PQFP. The tables in this section provide a description of the pins and their respective signal definitions.

Table 1 lists the tables in this section. Figure 2 shows the 21140 pinout.

Table 1 Index to Pinout Tables

For this information . . .	Refer to . . .
Logic signals	Table 2
Power pins	Table 3
Functional signals description	Table 4
Input pins	Table 5
Output pins	Table 6
Input/output pins	Table 7
Open drain pins	Table 8
Signal functions	Table 9

Figure 2 DECchip 21140 Pinout Diagram (Top View)



2.1 Signal Reference Tables

Table 2 provides an alphabetical list of the 21140 logic names and their pin numbers. Table 3 provides a list of the 21140 power pin numbers.

Table 2 Logic Signals

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
ad<00>	72	ad<24>	20	int_l	1
ad<01>	71	ad<25>	19	irdy_l	40
ad<02>	69	ad<26>	17	mii_clsn	112
ad<03>	68	ad<27>	16	mii_crs	113
ad<04>	66	ad<28>	14	mii_dv	111
ad<05>	65	ad<29>	13	mii_err	110
ad<06>	63	ad<30>	11	mii_mdc	106
ad<07>	62	ad<31>	10	mii_mdio	105
ad<08>	60	c_be_l<00>	61	mii/srl	133
ad<09>	58	c_be_l<01>	48	mii/sym_rclk	114
ad<10>	57	c_be_l<02>	38	mii/sym_rxd<00>	115
ad<11>	55	c_be_l<03>	21	mii/sym_rxd<01>	116
ad<12>	54	devsel_l	42	mii/sym_rxd<02>	117
ad<13>	52	frame_l	39	mii/sym_rxd<03>	118
ad<14>	51	gep<00>	80	mii/sym_tclk	123
ad<15>	50	gep<01>	81	mii/sym_txd<00>	126
ad<16>	35	gep<02>	82	mii/sym_txd<01>	127
ad<17>	34	gep<03>	83	mii/sym_txd<02>	130
ad<18>	30	gep<04>	86	mii/sym_txd<03>	131
ad<19>	29	gep<05>	87	mii/sym_txen	125
ad<20>	27	gep<06>	88	nc	101
ad<21>	26	gep<07>	89	nc	102
ad<22>	25	gnt_l	7	nc	103
ad<23>	24	idsel	22	nc	104

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Table 2 (Cont.) Logic Signals

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
par	47	rsv_vss<06>	99	srl_tclk	139
pci_clk	5	rsv_vss<07>	100	srl_txd	138
perr_l	45	sd	109	srl_txen	140
rcv_match	122	serr_l	46	stop_l	43
req_l	8	sr_ck	78	sym_link	124
rst_l	2	sr_cs	79	sym_rxd<04>	119
rsv_vss<00>	91	sr_di	77	sym_txd<04>	132
rsv_vss<01>	92	sr_do	76	tck	141
rsv_vss<02>	93	srl_clsn	134	tdi	143
rsv_vss<03>	94	srl_rclk	137	tdo	144
rsv_vss<04>	95	srl_rxd	135	tms	142
rsv_vss<05>	96	srl_rxen	136	trdy_l	41

Table 3 Power Pins

Signal	Pin Numbers	Signal	Pin Numbers
vdd (3.3 V)	3, 6, 18, 28, 31, 44, 56, 67, 75, 85, 98, 107, 121, 129	vss (GND)	4, 9, 12, 15, 23, 32, 33, 36, 37, 49, 53, 59, 64, 70, 74, 84, 90, 97, 108, 120, 128
vdd_clamp (5 V)	73		

Table 4 provides a functional description of each of the 21140 signals. These signals are listed alphabetically. The functional grouping of each pin is listed in Section 2.3.

The following terms describe the 21140 pinout:

- **Address phase**

  Address and appropriate bus commands are driven during this cycle.

- **Data phase**

  Data and the appropriate byte enable codes are driven during this cycle.

- **_l**

  All pin names with the _l suffix are asserted low.

The following abbreviations are used in Table 4.

I = Input
O = Output
I/O = Input/output
O/D = Open drain
P = Power

Table 4 Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
ad<31:00>	I/O	See Table 2.	32-bit PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, the address bits contain a physical address (32 bits). During subsequent clock cycles, these same lines contain data (32 bits). A 21140 bus transaction consists of an address phase followed by one or more data phases. The 21140 supports both read and write bursts (in master operation only). Little and big endian byte ordering can be used.

(continued on next page)

Table 4 (Cont.) Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
c_be_l<03:00>	I/O	See Table 2.	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, these four bits provide the bus command. During the data phase, these four bits provide the byte enable. The byte enable determines which byte lines carry valid data. For example, bit 0 applies to byte 0, and bit 3 applies to byte 3.
devsel_l	I/O	42	Device select is asserted by the target of the current bus access. When the 21140 is the initiator of the current bus access, it expects the target to assert **devsel_l** within 5 bus cycles, confirming the access. If the target does not assert **devsel_l** within the required bus cycles, the 21140 aborts the cycle. To meet the timing requirements, the 21140 asserts this signal in a medium speed (within 2 bus cycles).
frame_l	I/O	39	The **frame_l** signal is driven by the 21140 (bus master) to indicate the beginning and duration of an access. The **frame_l** signal asserts to indicate the beginning of a bus transaction. While **frame_l** is asserted, data transfers continue. The **frame_l** signal deasserts to indicate that the next data phase is the final data phase transaction.
gep<07:00>	I/O	See Table 2.	General-purpose pins can be used by software as either status pins or control pins. These pins can be configured by software to perform either input or output functions.
gnt_l	I	7	Bus grant asserts to indicate to the 21140 that access to the bus is granted.
idsel	I	22	Initialization device select asserts to indicate that the host is issuing a configuration cycle to the 21140.

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Table 4 (Cont.) Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
int_l	O/D	1	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. Interrupt request deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5 and the host doesn't clear all input bits, the 21140 deasserts **int_l** for one cycle to support edge-triggered systems. This pin must be pulled up by an external resistor.
irdy_l	I/O	40	Initiator ready indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock when both **irdy_l** and target ready **trdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21140 is the bus master, **irdy_l** is asserted during write operations to indicate that valid data is present on the 32-bit **ad** lines. During read operations, the 21140 asserts **irdy_l** to indicate that it is ready to accept data.
mii_clsn	I	112	Collision detected is asserted when detected by an external physical layer protocol (PHY) device.
mii_crs	I	113	Carrier sense is asserted by the PHY when the media is active.
mii_dv	I	111	Data valid is asserted by an external PHY when receive data is present on the **mii/sym_rxd** lines and deasserted at the end of the packet. This signal should be synchronized with the **mii/sym_rclk** signal.

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Table 4 (Cont.) Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
mii_err	I	110	Receive error asserts when a data decoding error is detected by an external PHY device. This signal is synchronized to **mii/sym_rclk** and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the cyclic redundancy check (CRC) error bit in the receive descriptor (RDES0).
mii_mdc	O	106	MII management data clock is sourced by the 21140 to the PHY devices as a timing reference for the transfer of information on the **mii_mdio** signal.
mii_mdio	I/O	105	MII management data input/output transfers control information and status between the PHY and the 21140.
mii/srl	O	133	Indicates the selected port: SRL or MII/SYM. When asserted, the MII/SYM port is active. When deasserted, the SRL port is active.
mii/sym_rclk	I	114	Supports either the 25-MHz or 2.5-MHz receive clock. This clock is recovered by the PHY.
mii/sym_ rxd<03:00>	I	See Table 2.	Four parallel receive data lines when MII mode is selected. This data is driven by an external PHY that attached the media and should be synchronized with the **mii/sym_rclk** signal.
mii/sym_tclk	I	123	Supports the 25-MHz or 2.5-MHz transmit clock supplied by the external PMD device. This clock should always be active.
mii/sym_ txd<03:00>	O	See Table 2.	Four parallel transmit data lines. This data is synchronized to the assertion of the **mii/sym_tclk** signal and is latched by the external PHY on the rising edge of the **mii/sym_tclk** signal.
mii/sym_txen	O	125	Transmit enable signals that the transmit is active to an external PHY device. This signal is ignored in PCS mode (CSR6<23>).

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Table 4 (Cont.) Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
nc	O	101	No connection.
nc	O	102	No connection.
nc	O	103	No connection.
nc	O	104	No connection.
par	I/O	47	Parity is calculated by the 21140 as an even parity bit for the 32-bit **ad** and 4-bit **c_be_l** lines. During address and data phases, parity is calculated on all the **ad** and **c_be_l** lines whether or not any of these lines carry meaningful information.
pci_clk	I	5	The clock provides the timing for the 21140 related PCI bus transactions. All the bus signals are sampled on the rising edge of **pci_clk**. The clock frequency range is between 25 MHz and 33 MHz.
perr_l	I/O	45	Parity error asserts when a data parity error is detected. When the 21140 is the bus master and a parity error is detected, the 21140 asserts both CSR5 bit 13 (system error) and CFCS bit 8 (**serr_l** enable). Next, it completes the current data burst transaction, then stops operation. After the host clears the system error, the 21140 continues its operation. When the 21140 is the bus target and a parity error is detected, the 21140 asserts **perr_l**. This pin must be pulled up by an external resistor.
rcv_match	O	122	Receive match indication is asserted when a received packet has passed address recognition.
req_l	O	8	Bus request is asserted by the 21140 to indicate to the bus arbiter that it wants to use the bus.

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Table 4 (Cont.) Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
rst_l	I	2	Resets the 21140 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI output pins are put into tristate and all PCI O/D signals are floated.
rsv_vss<07:00>	I	See Table 2.	Reserved. Must be tied to **vss**.
sd	I	109	Signal detect indication supplied by an external physical layer medium dependent (PMD) device.
serr_l	I/O	46	If an address parity error is detected and CFCS bit 31 (detected parity error) is enabled, 21140 asserts both **serr_l** (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address. This pin must be pulled up by an external resistor.
sr_ck	O	78	Serial ROM clock signal.
sr_cs	O	79	Serial ROM chip-select signal.
sr_di	O	77	Serial ROM data-in signal.
sr_do	I	76	Serial ROM data-out signal.
srl_clsn	I	134	Collision detect signals a collision occurrence on the Ethernet cable to the 21140. It may be asserted and deasserted asynchronously by the external ENDEC to the receive clock.
srl_rclk	I	137	Receive clock carries the recovered receive clock supplied by an external ENDEC. During idle periods, **srl_rclk** may be inactive.
srl_rxd	I	135	Receive data carries the input receive data from the external ENDEC. The incoming data should be synchronous with the **srl_rclk** signal.

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Table 4 (Cont.) Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
srl_rxen	I	136	Receive enable signals activity on the Ethernet cable to the 21140. It is asserted when receive data is present on the Ethernet cable and deasserted at the end of a frame. It may be asserted and deasserted asynchronously to the receive clock (**srl_rclk**) by the external ENDEC.
srl_tclk	I	139	Transmit clock carries the transmit clock supplied by an external ENDEC. This clock must always be active (even during reset).
srl_txd	O	138	Transmit data carries the serial output data from the 21140. This data is synchronized to the **srl_tclk** signal.
srl_txen	O	140	Transmit enable signals an external ENDEC that the 21140 transmit is in progress.
stop_l	I/O	43	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The 21140 responds to the assertion of **stop_l** when it is the bus master, either to disconnect, retry, or abort.
sym_link	O	124	Indicates that the descrambler is locked to the input data signal.
sym_rxd<04>	I	119	Receive data, together with the four receive lines **mii/sym_rxd<03:00>**, provide five parallel lines of data in symbol form for use in PCS mode (100BASE-T, CSR6<23>). This data is driven by an external PMD device and should be synchronized to the **mii/sym_rclk** signal.
sym_txd<04>	O	132	Transmit data, together with the four transmit lines **mii/sym_txd<03:00>**, provide five parallel lines of data in symbol form for use in PCS mode (100Base-T, CSR6<23>). This data is synchronized on the rising edge of the **mii/sym_tclk** signal.

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Table 4 (Cont.) Functional Description of DECchip 21140 Signals

Signal	Type	Pin Number	Description
tck	I	141	JTAG clock shifts state information and test data into and out of the 21140 during JTAG test operations. This pin should not be left unconnected.
tdi	I	143	JTAG data in is used to serially shift test data and instructions into the 21140 during JTAG test operations. This pin should not be left unconnected.
tdo	O	144	JTAG data out is used to serially shift test data and instructions out of the 21140 during JTAG test operations.
tms	I	142	JTAG test mode select controls the state operation of JTAG testing in the 21140. This pin should not be left unconnected.
trdy_l	I/O	41	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both **trdy_l** and **irdy_l** are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21140 is the bus master, target ready is asserted by the bus slave on the read operation indicating that valid data is present on the **ad** lines. During a write cycle, it indicates that the target is prepared to accept data.
vdd	P	See Table 3.	3.3-volt supply input voltage.
vdd_clamp	P	73	5-volt power.
vss	P	See Table 3.	Ground pins.

2.2 Pin Tables

This section contains four types of pin tables:

- Table 5 lists the input pins.
- Table 6 lists the output pins.
- Table 7 lists the input/output pins.
- Table 8 lists the open drain pins.

Table 5 Input Pins

Signal	Active Level	Signal	Active Level
gnt_l	Low	sd	High
idsel	High	sr_do	High
mii_clsn	High	srl_clsn	High
mii_crs	High	srl_rclk	—
mii_dv	High	srl_rxd	–
mii_err	High	srl_rxen	High
mii/sym_rclk	–	srl_tclk	—
mii/sym_rxd<03:00>	–	sym_rxd<04>	—
mii/sym_tclk	–	tck	—
pci_clk	–	tdi	—
rst_l	Low	tms	High
rsv_vss<07:00>	–		

Table 6 Output Pins

Signal	Active Level	Signal	Active Level
mii_mdc	–	sr_cs	High
mii/srl	–	sr_di	High
mii/sym_txd<03:00>	–	srl_txd	–
mii/sym_txen	High	srl_txen	High
nc	–	sym_link	High
rcv_match	High	sym_txd<04>	–
req_l	Low	tdo	High
sr_ck	–		

Table 7 Input/Output Pins

Signal	Active Level	Signal	Active Level
ad<31:00>	—	mii_mdio	—
c_be_l<03:00>	Low	par	—
devsel_l	Low	perr_l	Low
frame_l	Low	serr_l	Low
gep<07:00>	—	stop_l	Low
irdy_l	Low	trdy_l	Low

Table 8 Open Drain Pins

Signal	Active Level
int_l	Low

2.3 Signal Grouping by Function

Table 9 lists the signals according to their interface function.

Table 9 Signal Functions

Interface	Function	Signal
PCI	Address and data	ad<31:00>, par
	Arbitration	gnt_l, req_l
	Bus command and byte enable	c_be_l<03:00>
	Device select	devsel_l, idsel
	Error reporting	perr_l, serr_l
	Interrupt	int_l
	System	pci_clk, rst_l
	Control signals	frame_l, stop_l, irdy_l, trdy_l
MII/symbol	Transmit data lines	mii/sym_txd<03:00>
Network port	Receive data lines	mii/sym_rxd<03:00>
	Transmit, receive clocks	mii/sym_tclk, mii/sym_rclk
	SYM mode	sym_rxd<04>, sym_txd<04>
	Signal detection	sd
	Transmit enable	mii/sym_txen
	Collision detect	mii_clsn
	Error reporting	mii_err
	Data control	mii_dv, mii_crs
	MII management data clock	mii_mdc
	MII management data input/output	mii_mdio
Serial port	Transmit and receive data	srl_txd, srl_rxd
	Transmit control	srl_txen, srl_tclk
	Receive control	srl_rxen, srl_rclk
	Collision detect	srl_clsn
Miscellaneous	LED indicators	rcv_match, sym_link
	General-purpose pins	gep<07:00>
	MII/SYM and serial port select	mii_srl

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Table 9 (Cont.)   Signal Functions

Interface	Function	Signal
Test access port	JTAG test operations	tck, tdi, tdo, tms
Ethernet ID port	Address ROM	sr_ck, sr_cs, sr_di, sr_do
Power	3.3-volt and 5-volt supply input	vdd, vdd_clamp
	Ground	vss

3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications of the 21140.

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21140. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21140.

3.1 Voltage Limit Ratings

Table 10 lists the voltage limit ratings.

Table 10 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.135 V	+3.465 V
vdd_clamp (5.0 V)	+4.75 V	+5.25 V
ESD protection voltage	–	2000 V

3.2 Temperature Limit Ratings

Table 11 lists the temperature limit ratings.

Table 11 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	70°C

3.3 Supply Current and Power Dissipation

The values in Table 12 are estimates based on a PCI clock frequency of 33 MHz and a network data rate of 10-Mb/s for SRL and 100-Mb/s for MII.

Table 12 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	vdd =3.465 V, Ta=70°C	160	210	mA
Power	vdd=3.465 V, Ta=70°C	0.52	0.72	W

3.3.1 PCI I/O Voltage Specifications

The 21140 meets the I/O voltage specifications listed in Table 13.

Table 13 I/O Voltage Specifications for 5.0-Volt Environment

Category	PCI I/O	PCI Output	PCI Input
Vil	O.8 V	–	0.8 V
Vih	2.0 V	–	2.0 V
Vol[1]	0.55 V	0.55 V	–
Voh	2.4 V	2.4 V	–
Ioh	–2 mA	–2 mA	–
Ioz	+/–70 µA	+/–70 µA	–
Max Vin	vdd_clamp + 0.5 V	–	vdd_clamp + 0.5 V

[1]Signals without pullup resistors must have 3 milliamps low output current. Signals requiring pullup resistors (including **frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l, and perr_l**) must have 6 milliamps.

3.3.2 PCI Reset

PCI reset (**pci_rst**) is an asynchronous signal that must be active for at least 10 active PCI clock (**pci_clk**) cycles. Figure 3 shows the PCI reset timing characteristics, and Table 14 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

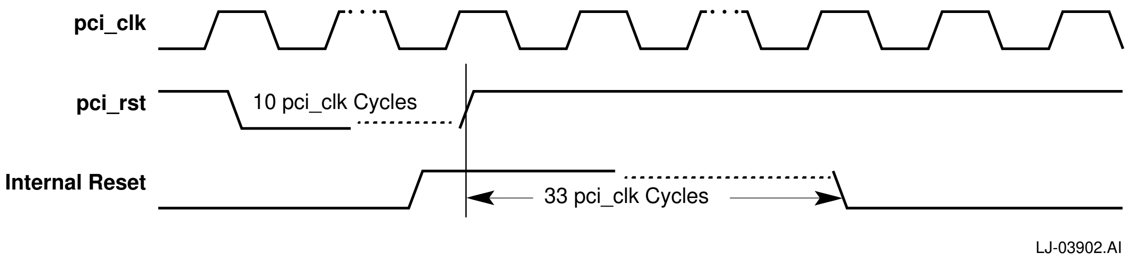


Table 14 PCI Reset Timing

Symbol	Parameter	Minimum	Maximum	Conditions
Trst	**pci_rst** pulse width	10*Tcycle	Not applicable	**pci_clk** active

3.3.3 PCI Clock Specifications

The clock frequency range for the PCI is between 25 MHz and 33 MHz. Figure 4 shows the PCI clock specification timing characteristics, and Table 15 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Specifications Timing Diagram

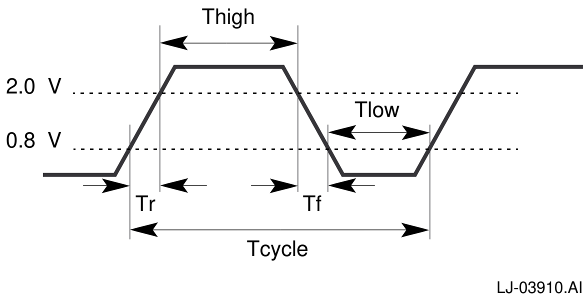


Table 15 PCI Clock Specifications

Symbol	Parameter	Minimum	Maximum	Notes
Tcycle	Cycle time	30 ns	40 ns	–
Thigh	pci_clk high time	12 ns	24 ns	At 2 V
Tlow	pci_clk low time	12 ns	24 ns	At 0.8 V
Tr/Tf[1]	pci_clk slew rate	1 V/ns	4 V/ns	–

[1]Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

3.3.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 16 lists the other PCI signals. This timing is identical to the timing for the general-purpose register signals.

Figure 5 Timing Diagram for Other PCI Signals

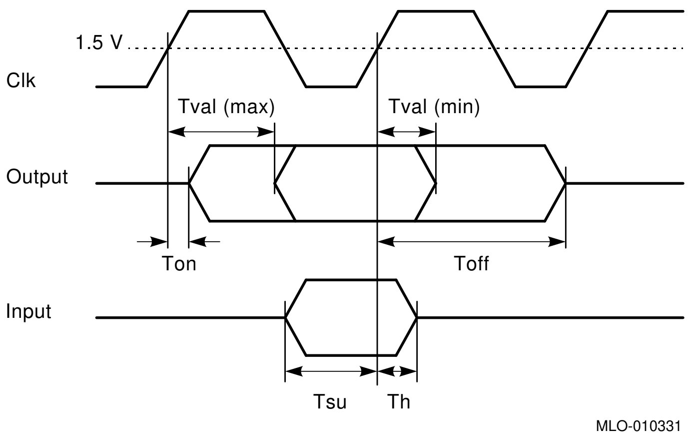


Table 16 Other PCI Signals

Symbol	Parameter	Minimum	Maximum	Conditions
Tval	clk-to-signal valid delay	2 ns	11 ns	Cload = 50 pF
Ton[1]	Float-to-active delay from clk	2 ns	–	–
Toff[1]	Active-to-float delay from clk	–	28 ns	–
Tsu	Input signal valid setup time before clk	7 ns	–	–
Th	Input signal hold time from clk	0 ns	–	–
Tr[1]	Unloaded output rise time	–	2 ns	0.4 V to 2.4 V
Tf[1]	Unloaded output fall time	–	2 ns	2.4 V to 0.4 V

[1]Parameter design guarantee.

3.4 Serial and MII Interface Specifications

Table 17 lists the specifications for the serial and MII interfaces.

Table 17 Serial and MII Interface Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4mA	2.4	–	V
V_{ol}	Output low voltage	I_{ol} = 4mA	–	0.4	V
V_{ih}	Input high voltage	–	2.0	–	V
V_{il}	Input low voltage	–	–	0.8	V
I_{in}	Input current	$V_{in} = V_{cc}$ or V_{ss}	–10.0	10.0	µA
I_{oz}	Maximum tristate output leakage current	$V_{in} = V_{dd}$ or V_{ss}	–10.0	10.0	µA

3.5 Serial Port Timing

This section describes the serial port timing limits.

3.5.1 Serial 10-Mb/s Timing—Transmit

Figure 6 shows the serial port transmit timing characteristics, and Table 18 lists the serial port transmit timing limits.

Figure 6 Serial Port Timing Diagram—Transmit

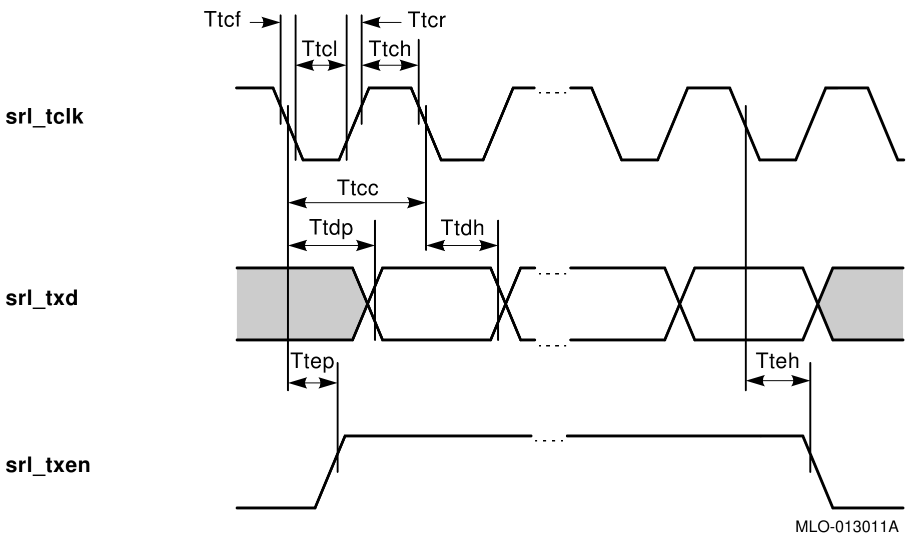


Table 18 Serial Port Timing—Transmit

Symbol	Definition	Minimum	Maximum	Units
Ttcl	**srl_tclk** low time	45	55	ns
Ttch	**srl_tclk** high time	45	55	ns
Ttcr[1]	**srl_tclk** rise time	–	8	ns
Ttcf[1]	**srl_tclk** fall time	–	8	ns
Ttdp	**srl_tclk** fall time to **srl_txd** valid	–	40	ns
Ttdh	**srl_txd** hold after **srl_tclk** fall time	5	–	ns
Ttep	**srl_tclk** fall time to **srl_txen** valid	–	40	ns
Tteh	**srl_txen** hold after **srl_tclk** fall time	5	–	ns

[1]Parameter design guarantee.

3.5.2 Serial 10-Mb/s Timing—Collision

Figure 7 shows the serial port collision timing characteristics, and Table 19 lists the serial port collision timing limit.

Figure 7 Serial Port Timing Diagram—Collision

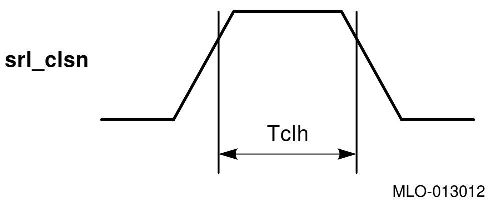


Table 19 Serial Port Timing—Collision

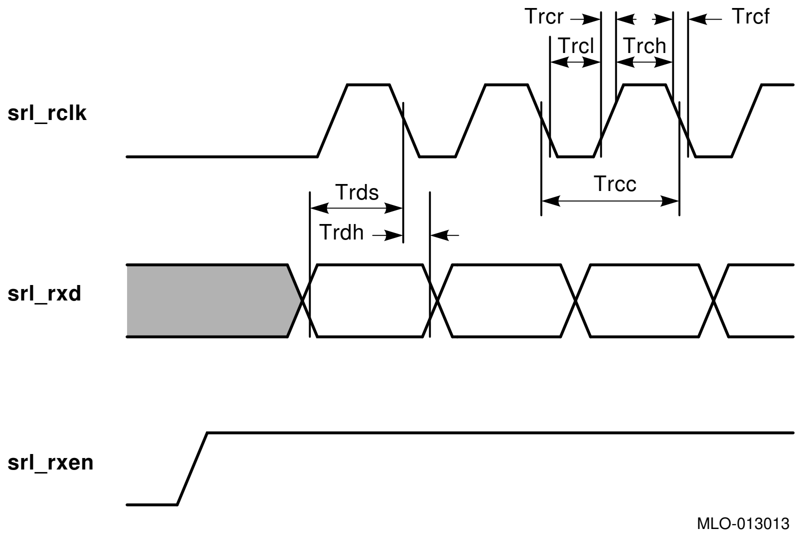
Symbol	Definition	Minimum	Maximum	Units
Tclh[1]	**srl_clsn** high time	20	–	ns

[1]Parameter design guarantee.

3.5.3 Serial 10-Mb/s Timing—Receive, Start of Packet

Figure 8 shows the serial port timing characteristics in receive mode, start of packet; and Table 20 lists the serial port timing limits in receive mode, start of packet.

Figure 8 Serial Port Timing Diagram—Receive, Start of Packet



3.5.4 Serial 10-Mb/s Timing—Receive, End of Packet

Figure 9 shows the serial port timing characteristics in receive mode, end of packet; and Table 20 lists the serial port timing limits in receive mode, end of packet.

Figure 9 Serial Port Timing Diagram—Receive, End of Packet

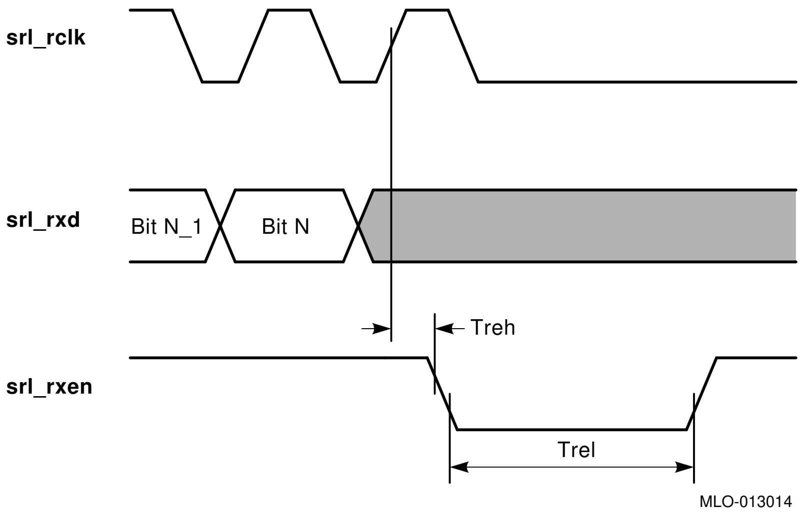


Table 20 Serial Port Timing—Receive, Start and End of Packet

Symbol	Definition	Minimum	Maximum	Units
Trcc	**srl_rclk** cycle time	85	118	ns
Trcl	**srl_rclk** low time	38	80	ns
Trch	**srl_rclk** high time	38	80	ns
Trcr[1]	**srl_rclk** rise time	–	8	ns
Trcf[1]	**srl_rclk** fall time	–	8	ns
Trds	**srl_rxd** setup to **srl_rclk** fall time	10	–	ns
Trdh	**srl_rxd** hold after **srl_rclk** fall time	5	–	ns
Trel	**srl_rxen** low time	120	–	ns
Treh	**srl_rxen** hold after **srl_rclk** rise time	40	–	ns

[1]Parameter design guarantee.

3.6 MII Port Timing

This section describes the MII port timing limits.

3.6.1 MII 100-Mb/s Timing—Transmit

Figure 10 shows the MII port transmit timing characteristics, and Table 21 lists the MII port transmit timing limits.

Figure 10 MII Port Timing Diagram—Transmit

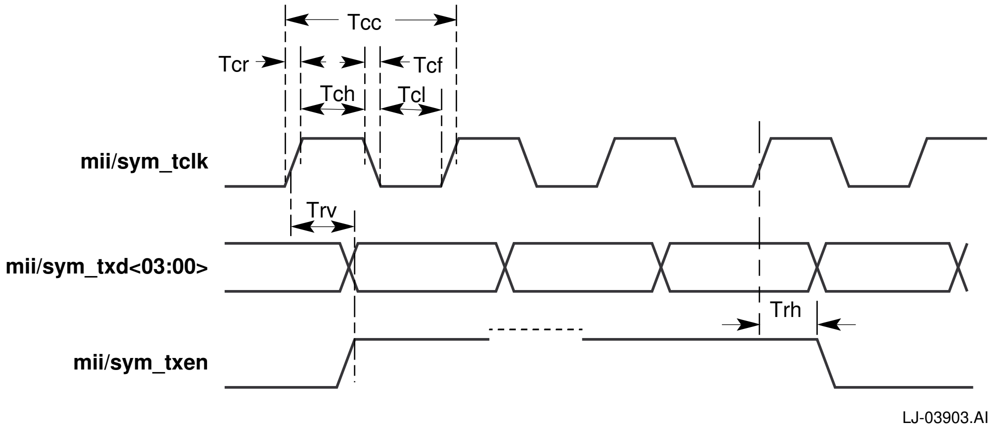


Table 21 MII Port Timing—Transmit

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc[1]	**mii/sym_tclk** cycle time	–	40	–	ns
Tch	**mii/sym_tclk** high time	14	–	26	ns
Tcl	**mii/sym_tclk** low time	14	–	26	ns
Tcr	**mii/sym_tclk** rise time	–	8	–	ns
Tcf	**mii/sym_tclk** fall time	–	8	–	ns
Trv[2]	**mii/sym_tclk** rise to **mii/sym_txen** valid time or **mii/sym_tclk** rise to **mii/sym_txd** valid time	–	–	16	ns
Trh	**mii/sym_txen** hold after **mii/sym_tclk** rise time	5	–	–	ns

[1]+/– 100 parts per million.

[2]Outputs transmit data (**mii/sym_txd**) and transmit enable (**mii/sym_txen**) are driven internally from the rising edge of **mii/sym_tclk**.

3.6.2 MII 100-Mb/s Timing—Receive

Figure 11 shows the MII port receive timing characteristics, and Table 22 lists the MII port receive timing limits.

Figure 11 MII Port Timing Diagram—Receive

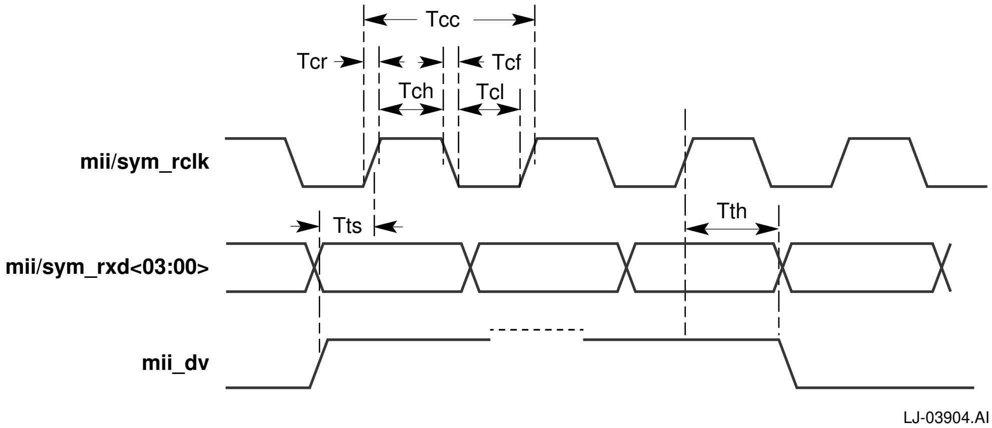


Table 22 MII Port Timing—Receive

Symbol	Definition	Minimum	Typical	Maximum	Units
Tcc	**mii/sym_rclk** cycle time	–	40	–	ns
Tch	**mii/sym_rclk** high time	14	–	26	ns
Tcl	**mii/sym_rclk** low time	14	–	26	ns
Tcr	**mii/sym_rclk** rise time	–	8	–	ns
Tcf	**mii/sym_rclk** fall time	–	8	–	ns
Tts[1]	**mii/sym_rxd** setup (both rise and fall transactions) to **mii/sym_rclk** rise time or **mii_dv** setup (both rise and fall transactions) to **mii/sym_rclk** rise time	10	–	–	ns
Tth	**mii/sym_rxd** hold (both rise and fall transactions) after **mii/sym_rclk** rise time or **mii_dv** hold (both rise and fall transactions) after **mii/sym_rclk** rise time	10	–	–	ns

[1]Inputs receive data (**mii/sym_rxd**) and data valid (**mii_dv**) are latched internally on the rising edge of **mii/sym_rclk**.

3.6.3 MII 100-Mb/s Timing—Signal Detect

Figure 12 shows the MII port signal detect timing characteristics, and Table 23 lists the MII port signal detect timing limits.

Figure 12 MII Port Timing Diagram—Signal Detect

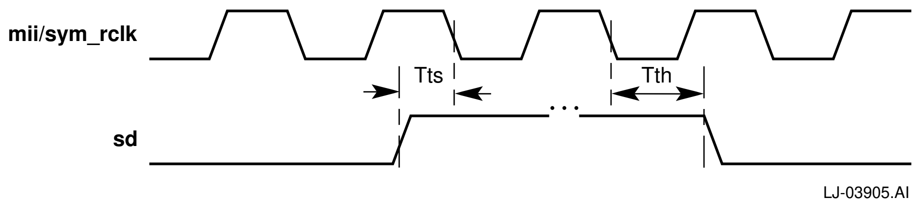


Table 23 MII Port Timing—Signal Detect

Symbol	Definition	Minimum	Maximum	Units
Tts[1]	**sd** setup (both rise and fall transactions) to **mii/sym_rclk** fall time	10	–	ns
Tth[1]	**sd** hold (both rise and fall transactions) after **mii/sym_rclk** fall time	12	–	ns

[1]Input signal detect (**sd**) is latched internally on the falling edge of **mii/sym_rclk**.

3.6.4 MII 100-Mb/s Timing—Receive Error

Figure 13 shows the MII port receive error timing characteristics, and Table 24 lists the MII port receive error timing limits.

Figure 13 MII Port Timing Diagram—Receive Error

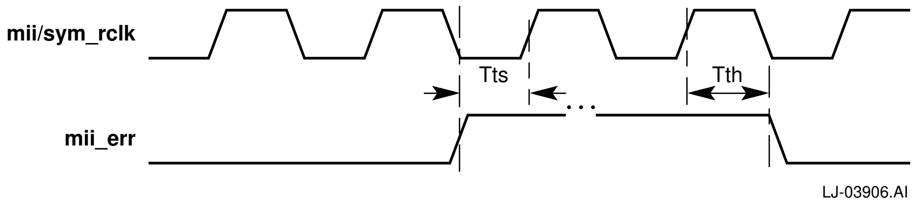


Table 24 MII Port Timing—Receive Error

Symbol	Definition	Minimum	Maximum	Units
Tts[1]	**mii_err** setup (both rise and fall transactions) to **mii/sym_rclk** rise time	10	–	ns
Tth[1]	**mii_err** hold (both rise and fall transactions) after **mii/sym_rclk** rise time	10	–	ns

[1]Input receive error (**mii_err**) is latched internally on the rising edge of **mii/sym_rclk**.

3.6.5 MII 100-Mb/s Timing—Carrier Sense and Collision

Figure 14 shows the MII port carrier sense and collision timing characteristics, and Table 25 lists the MII port carrier sense and collision timing limits.

Figure 14 MII Port Timing Diagram—Carrier Sense and Collision

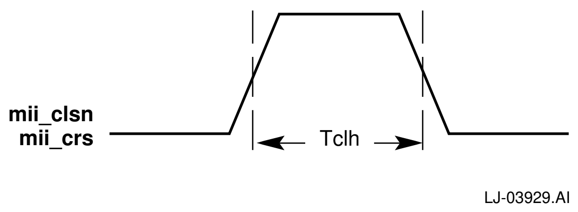


Table 25 MII Port Timing—Carrier Sense and Collision

Symbol	Definition	Minimum	Maximum	Units
Tclh	**mii_crs**, **mii_clsn** high time	20	–	ns

3.7 Ethernet ID Port Timing

Figure 15 shows the Ethernet ID port timing, and Table 26 lists the characteristics. This timing is identical to the timing for the MII management signals (**mii_mdio** and **mii_mdc**).

Figure 15 Ethernet ID Port Timing Diagram

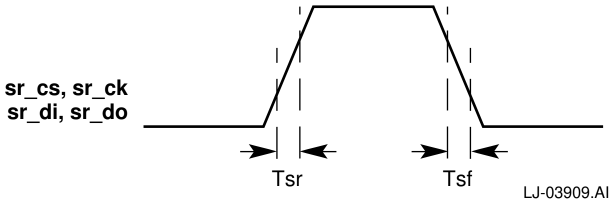


Table 26 Ethernet ID Port Timing Characteristics

Symbol	Definition	Minimum	Maximum	Units
Tsr	Rise time	–	10	ns
Tsf	Fall time	–	10	ns

3.8 Boot ROM Port Timing

The boot ROM port is not implemented in this release.

3.9 JTAG Boundary Scan Timing

Figure 16 shows the JTAG boundary scan timing, and Table 27 lists the interface signal timing relationships.

Figure 16 JTAG Boundary Scan Timing Diagram

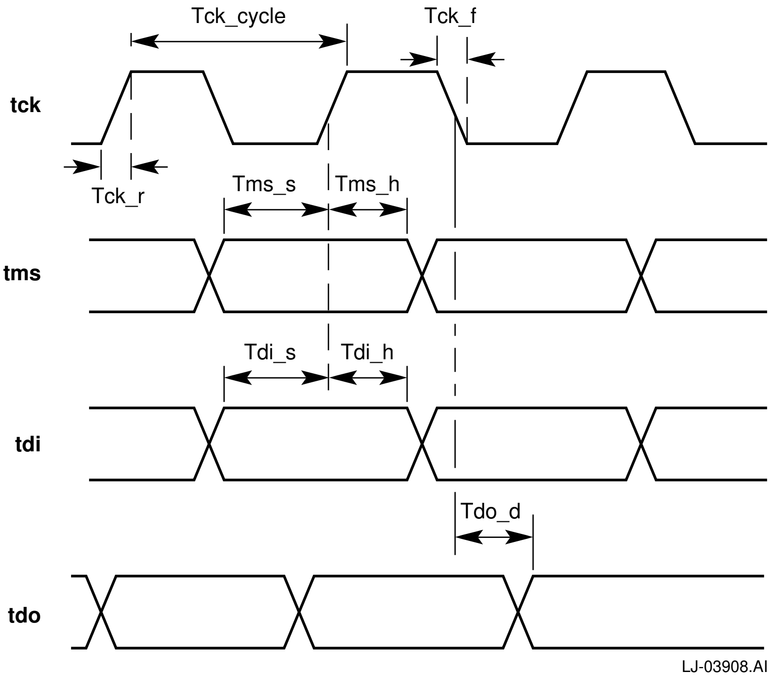


Table 27 JTAG Interface Signal Timing Relationships

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	**tms** setup time	20	–	ns
Tms_h	**tms** hold time	5	–	ns
Tdi_s	**tdi** setup time	20	–	ns
Tdi_h	**tdi** hold time	5	–	ns
Tdo_d	**tdo** delay time	–	20	ns
Tck_r[1]	**tck** rise time	–	3	ns
Tck_f[1]	**tck** fall time	–	3	ns
Tck_cycle	**tck** cycle time	90	–	ns

[1]Parameter design guarantee.

4 Mechanical Specifications

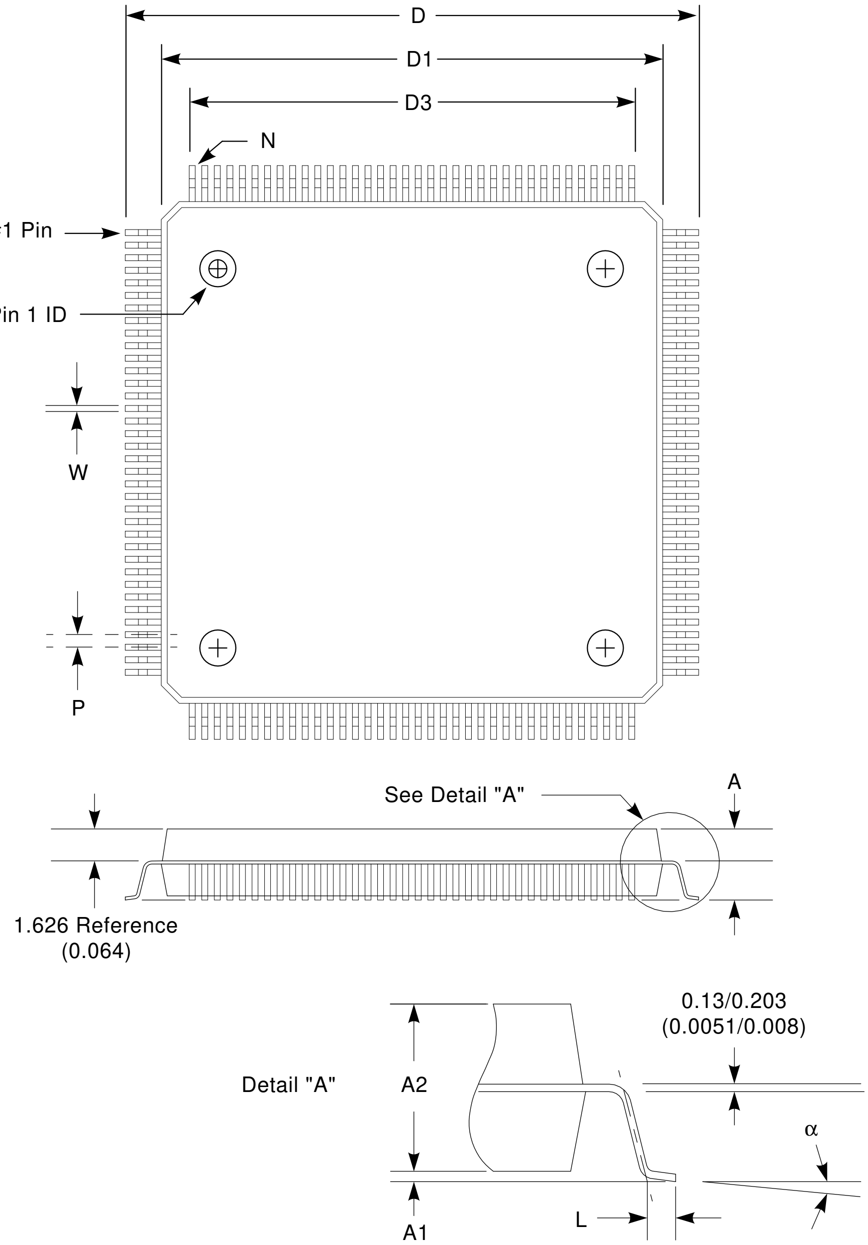
The 21140 is contained in a 144-pin plastic quad flat pack (PQFP). Table 28 lists the mechanical specifications, and Figure 17 shows the mechanical layout of the 21140.

Table 28 Mechanical Specifications

Item	Minimum[1]	Nominal[1]	Maximum[1]
A	–	–	4.07
A1	0.25	–	–
A2	3.17	3.37	3.67
D	–	31.20 BSC	–
D1	–	28.00 BSC	–
D3	22.75 Reference	22.75 Reference	22.75 Reference
L	0.65	0.80	1.00
N	–	144	–
P	0.65 BSC	0.65 BSC	0.65 BSC
W	0.22	0.30	0.38
α	0°	–	7°

[1] All dimensions (except α) are in millimeters.

Figure 17 Mechanical Layout of the DECchip 21140



Note: All dimensions are in millimeters.

MLO-013023

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